REMARKS:

I. Status of the Application.

Following the above amendments, claims 1 – 31, and 33 – 105 are pending.

In the October 19, 2004 Office Action (the "Office Action"), claims 1 – 105 were rejected under Sections 102(b) as anticipated (Office Action Points 2 – 18) and under Section 103(a) or obvious (Office Action Points 19 – 26) based on a single reference, Kopp et al. U.S. Patent No. 5,450,557 ("Kopp" or the "Kopp reference").

In this response, Applicants have amended claims 1 – 3, 7 – 11, 19, 21, 26, 31, 35, 36, 40 – 42, 44, 45, 47 – 51, 53, 58, 60 – 62, 64 – 74, 83 – 86, 88, 95, 96, 99, 101, 103, and 104, inclusive, and have canceled claim 32. Applicants respectfully traverse the rejection of claims claims 1 – 31 and 33 - 105 under Sections 102(b) and 103(a). Applicants respectfully request reconsideration of the pending claims in view of the foregoing amendments and the following remarks.

II. The Rejection of Claims 1 -31 and 33 – 105 Should Be Withdrawn.

In the October 19, 2004 Office Action, claims 1 – 105 were rejected under Sections 102(b) as anticipated (Office Action Points 2 – 18) and under Section 103(a) or obvious (Office Action Points 2 – 26) based on the Kopp reference. For the reasons stated below, Applicants respectfully traverse the rejection of claims 1 – 31 and 33 - 105 under Sections 102(b) and 103(a), and request that the Examiner withdraw the rejection of these claims. As discussed in greater detail below, the cited reference does not disclose all the limitations of the claimed invention and, in addition, teaches away from the claimed invention.

The Examiner should also note that the commonly assigned, first related application issued on December 28, 2004 as U. S. Patent No. 6,836,839 B2 (the related '839 patent). Various claims of the current application, as discussed below, are similar to and contain all of the limitations of certain allowed claims of the related '839 patent, and

further include limitations as to specific executable modules for providing configuration information and operand data.

The claimed invention provides a plurality of heterogeneous computational elements that are configurable and reconfigurable, through various levels of an interconnection network, to form a wide variety of functional or operational modes. At the various levels, such as at the lowest level of computational elements, the next level of computational units, and the higher level of matrices, the present invention utilizes "heterogeneity" at each such level. More specifically, computational elements having fixed and differing architectures are then combined in different sets, forming different, heterogeneous computational units, which are further combined to form heterogeneous matrices. (See, e.g., specification p. 12, ll. 1 – 20). This is in stark contrast to the prior art of reconfigurable or field programmable devices, which utilize arrays of identical, repeating sub-units.

The claimed invention also utilizes "nested" levels of configuration and reconfiguration of these heterogeneous computational elements, through multiple levels of interconnection networks. For example, a first matrix of heterogeneous computational elements having a first functionality is formed through a first interconnection network, and a second matrix of heterogeneous computational elements having a second functionality is formed through a second interconnection network. In turn, a third interconnection network is capable of configuring and reconfiguring these first and second matrices for a plurality of functional or operating modes, creating this multi-tiered or "nested" reconfigurability (see, e.g., specification p. 17, ll. 3 – 6; p. 18, ll. 2 – 26).

The configuring and reconfiguring of the heterogeneous computational elements through the interconnection network to provide various functional modes provides a truly dynamic integrated circuit, that not only adapts for existing systems but also for next generation systems (specification p. 13, ll. 11 – 24; p. 19, ll. 6 – 20).

The heterogeneous computational elements of the invention include fixed and differing IC architectures, such as fixed architectures for different functions such as memory, addition, multiplication, complex multiplication, subtraction, configuration, reconfiguration, control, input, output, and field programmability.

The configuration and reconfiguration of the plurality of heterogeneous computational elements is accomplished through an interconnection network, which changes the input and output connections of the plurality of heterogeneous computational elements, connecting and reconnecting these computational elements in different configurations to perform different functions at different times, in response to configuration information contained in a routable, executable module. In addition, particular heterogeneous computational elements are preselected and grouped into computational units, and further differentially grouped into matrices, for reconfigurable performance of a corresponding plurality of different functions. For example, one set of heterogeneous computational elements may be selected and configured to form a matrix for performance of an FFT, while a second and different set of heterogeneous computational elements may be selected and configured to form a matrix for bit manipulation, such as Viterbi decoding. The resulting reconfigurable matrices, using different mixes and layouts of these fixed and different computational elements, therefore have different architectures.

In order to control and time such configurations, the present invention utilizes executable modules which contain the corresponding *configuration information*, which are *selectively routable* over the interconnection network to selected groups of computational elements. In addition, these executable modules *contain operand data*, such as a data payload. It is respectfully submitted that the cited references, alone or in combination, do not disclose or suggest executable modules having these three separate features, namely, configuration information, routing information, and operand data. Rather, as discussed in greater detail below, the cited references only disclose use of an instruction provided on a dedicated, non-routable path, with data being separately provided on separate and dedicated, non-routable data paths.

Independent claims 1, 26, 31, 40, 64, 88, 99, 101, 103 and 104 have been amended to reflect these three novel features of the routable and executable modules of the present invention.

In addition, the various cited references do not utilize or disclose such routable and executable modules because they are directed to vastly different architectures. As illustrated in the related and issued U. S. Patent No. 6,836,839, the

heterogeneous computational elements having fixed and differing architectures, which are configurable and reconfigurable for multiple and different functions, of the claimed invention, are not present in the prior art. In addition, the prior art does not disclose using different mixes and layouts of these fixed and different computational elements, to form larger reconfigurable matrices, which are also heterogeneous. The prior art does not disclose or suggest the multi-tiered or "nested" reconfigurability of these heterogeneous computational elements through a plurality of interconnection networks. As a further consequence, such cited references do not disclose the routable and executable modules of the present invention.

The Kopp reference utilizes different processing elements connected to input and output registers, with multiplexers changing connections between the various registers, programmed through a very long word instruction directly provided to multiplexers using dedicated and separate programming lines (or connections), illustrated as the separate lines to the multiplexers in Figures 1b, 1c and 1d. Kopp does not utilize or suggest using an executable module which may be routed on shared configuration lines or interconnect. In addition, Kopp utilizes dedicated input data lines, and further does not disclose providing encapsulated operand data using an executable module, and further which also may be selectively routed on shared data lines or interconnect.

As a consequence, Kopp does not suggest or disclose either the routability of the executable modules of the present invention, and further does not disclose or suggest the encapsulation of operand data within the executable modules of the present invention. Indeed, using separate and dedicated, non-routable programming and input data lines, Kopp *teaches away* from the present invention. MPEP Section 2141.02. Such teaching away is the antithesis of art suggesting that a person of ordinary skill go in the claimed direction. See *In re Fine*, 873 F.2d 1071 (Fed. Cir. 1988). This teaching away from Applicants' invention is a *per se* and conclusive demonstration of lack of obviousness and a lack of anticipation.

Kopp also does not disclose or suggest other limitations of the various independent claims of the present invention, such as the configuration and reconfiguration of a plurality of heterogeneous computational elements, each having different fixed architectures, for different functions. Kopp also does not disclose or

suggest using different mixes and layouts of these fixed and different computational elements to form differing reconfigurable matrices for different functional and operational modes. Kopp also does not disclose or suggest the multi-tiered or "nested" reconfigurability of these heterogeneous computational elements through a plurality of interconnection networks.

The remaining independent claim 102 is also not disclosed or suggested by Kopp. More specifically, none of the cited references disclose not only an executable module containing both configuration information and data, but also where subsets of the plurality of heterogeneous computational elements are themselves configured for a controller operating mode and a memory operating mode.

As a consequence, the Kopp reference, alone or in combination with the other cited references (below), does not disclose or suggest all of the limitations of the independent claims of the present invention, such as the routable executable module containing routing information, configuration information, and operand data, of the independent claims. In addition, Kopp and the other references do not disclose the configuration and reconfiguration of a plurality of heterogeneous computational elements, each having different fixed architectures, for different functions, of the independent claims of the present invention. Moreover, the examiner has not presented any motivation, suggestion or teaching to combine Kopp with these other references (discussed below). Accordingly, no *prima facie* showing of potential anticipation or obviousness has been made, and any assertions to the contrary have been clearly rebutted. *In re Rouffet*, 149 F.3d 1350 (Fed. Cir. 1998); *In re Mills*, 916 F.2d 680 (Fed. Cir. 1990). The rejection of claims 1 – 31 and 33 - 105 as anticipated under Section 102 or obvious under Section 103(a), therefore, should be withdrawn.

III. The Other Cited References Do Not Disclose or Suggest The Claims of the Present Invention.

Wasson U.S. Patent 6,433,578 ("Wasson" or the "Wasson reference") utilizes a first, non-reconfigurable array of identical, repeating units of "structured data path logic", having dedicated (non-reconfigurable) routing, each having fixed data I/O and dedicated data busses. Specifically, each bit-specific sub-block receives inputs

(databus bits) from the immediately adjacent block, and the dedicated structured logic is not reconfigurable. Wasson Figures 12, 13 and 16, Col. 7, ll. 24 – 27, 54 – 55, and Wasson claim 1. A second, adjacent array of programmable, repeating units of identical unstructured control logic, similar to FPGA material (core cell, Figure 11), is also utilized to provide common control signals for the first array (Figures 8 and 10 and 11; Col. 6, ll. 17 – 22). A ring of programmable interconnect is also provided to the pads at the edge of the IC (Figures 15 and 16) for I/O (106) for programmable routing within the second, unstructured array, while the first, structured array utilizes dedicated, non-reconfigurable data bus routing directly to and from the I/O pads (Wasson Figure 16, 1204, and Col. 8, ll. 4-13). The reconfigurability of the architecture of the Wasson reference is, therefore, limited to the second, unstructured array having repeating units of identical, non-heterogeneous control logic.

As a consequence, Wasson also does not disclose or suggest all of the limitations of the independent claims of the present invention, such as the routable executable module containing routing information, configuration information and operand data, and the configuration and reconfiguration of a plurality of heterogeneous computational elements, each having different fixed architectures, for different functions. Instead, by utilizing a first, non-reconfigurable array of repeated and identical structured data path logic units, and a second, reconfigurable array of repeated and identical FPGA-like units, Wasson also teaches away from the present invention, particularly the multiple levels of heterogeneity employed in the present invention.

Harrison et al. U.S. Patent No. 5,963,048 generally discussed programming a programmable logic device having different functions. DeHon et al. U.S. Patent No. 5,956,518 generally discloses multi-bit processing units arranged in a configurable mesh. Wong et al. U.S. Patent No. 6,282,627 provides a standard processor with reconfigurable logic, with corresponding recompilation of software. None of these references disclose or suggest all of the limitations of the independent claims of the present invention, such as the routable executable module containing routing sequences, configuration information and operand data, and the configuration and reconfiguration of a plurality of heterogeneous computational elements, each having different fixed architectures, for different functions.

The remaining two references (Holtzman et al. U.S. Patent No. 6,760,587 and Walton et al. U.S. Patent no. 6,785,341) are generally in the fields of communications, and do not disclose or suggest all of the limitations of the independent claims of the present invention, such as the routable executable module containing routing sequences, configuration information and operand data, and the configuration and reconfiguration of a plurality of heterogeneous computational elements, each having different fixed architectures, for different functions.

IV. Other References Revealed In the Examinations of Other, Related Applications Also Do Not Disclose and Do Not Suggest All of the Limitations of the Claims of the Present Invention.

A. The Related '839 Patent:

Three main references were cited in the prosecution of the related '839 patent: Marshall et al. U.S. Patent No. 6,353,841 ("Marshall" or the "Marshall reference") in view of Bertolet et al. U.S. Patent No. 5,910,733 ("Bertolet" or the "Bertolet reference"), and in further view of Agrawal et al. U.S. Patent No. 5,889,816 ("Agrawal" or the "Agrawal reference").

With respect to the Marshall reference, Marshall merely discloses a repeating array of identical arithmetic logic units (ALUs) embedded in a switching fabric. These ALUs have the same inputs on every clock cycle. Marshall does not disclose or suggest all of the limitations of the independent claims of the present invention, such as the routable executable module containing routing sequences, configuration information and operand data, and the configuration and reconfiguration of a plurality of heterogeneous computational elements, each having different fixed architectures, for different functions. In addition, Marshall does not disclose or suggest the multi-tiered or "nested" reconfigurability of these heterogeneous computational elements through a plurality of interconnection networks. Using a repeating array of identical ALUs, therefore, the Marshall reference *teaches away* from the present invention.

The Bertolet reference also does not disclose the not disclose or suggest the routable executable module containing routing sequences, configuration information and operand data, and the configuration and reconfiguration of a plurality of

heterogeneous computational elements, each having different fixed architectures, for different functions. In addition, the Bertolet reference also does not disclose the not disclose or suggest the heterogeneity of computational elements, and the various different sets of heterogeneous computational elements selected to form heterogeneous and reconfigurable matrices, of the present invention. Indeed, the Bertolet reference merely discloses known FPGA material which is provided in different sizes or amounts (based on row and column width of the repeating array), and is otherwise a repetitive array of identical computational units (core cells), with all remaining elements being traditional and repetitive FPGA interconnect.

The Agrawal reference merely discloses a wireless adapter. The Agrawal reference, alone or in combination with the Marshall and Bertolet references, does not disclose or suggest all of the limitations of the independent or dependent claims discussed above.

B. The PCT Search Report for a First Related Application:

The PCT Search Report of one of the related, commonly assigned applications, U.S. Patent Application Serial No. 09/997,530, filed November 30, 2001, and its corresponding PCT/US02/37014, also disclosed Harrison et al. U.S. Patent No. 5,963,048 and Wong et al. U.S. Patent No. 6,282,627, discussed above, as not particularly relevant. The preliminary examination report found all 100 claims allowable. The examiner should note that these allowable claims are built upon and are very similar and highly related to the claims of the present invention. The USPTO has not yet provided a substantive office action on this second related application.

C. The US and PCT Search Reports for a Third Application:

The US and PCT Search Reports for a third commonly assigned applications, U.S. Patent Application Serial No. 09/871,049, filed May 31, 2001 and issued September 9, 2003 as US Patent No. 6,618,434, and its corresponding PCT/US02/16044, cited Ito U.S. Patent No. US 6,408,039 B1 (the "Ito patent" or the "Ito reference"). For a rake receiver for communication systems, the Ito patent provides a plurality of combination searcher and finger circuits (Fig. 1), which can operate in either

as searchers or multipath receivers (Col. 3, l. 46 – Col. 4, l. 8). As illustrated in Fig. 2 of the Ito patent, however, each of these functions is performed by separate, dedicated ASIC circuits, with the searcher mode utilizing despreader and signal strength calculator circuits, and with the finger mode utilizing the output of the despreader, along with different and separate dedicated ASIC circuits, namely, a delay lock loop, a phase calculator, a walsh despreader, and a phase equalizer (Col. 3, l. 51 – Col. 4, l. 19). The Ito patent uses these entirely different, dedicated circuits to perform either searching or path reception in all of the various embodiments disclosed. As a consequence, the Ito patent discloses using one set of dedicated ASIC circuits for searching, and another set of dedicated ASIC circuits for path reception, with each of these circuits repeatedly duplicated to form the multiple combination searcher/fingers. When one set of dedicated ASIC circuits is operational, the other set of dedicated ASIC circuits forming the combination searcher/finger is non-operational and quiescent.

The Ito patent merely discloses providing many additional, duplicative dedicated ASIC circuits for either searching or path reception, resulting in circuits which can be called to function as needed. Ito does not disclose or suggest all of the limitations of the independent claims of the present invention, such as the configuration and reconfiguration of a plurality of heterogeneous computational elements, each having different fixed architectures, for different functions. Ito also does not disclose or suggest the routable executable module of the present invention, containing routing sequences, configuration information and operand data, and the configuration and reconfiguration of a plurality of heterogeneous computational elements. As a consequence, the Ito patent does not disclose and does not suggest the claimed features of the present invention.

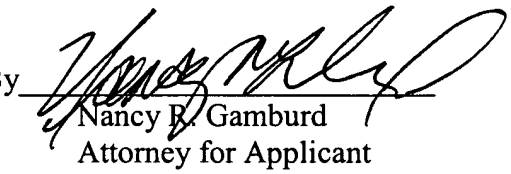
As a consequence, the cited references for this and related applications do not disclose and do not suggest the present invention. The present invention, therefore, is not anticipated and is not rendered obvious by these references under Sections 102 and 103, and the rejection of the claims should be withdrawn. In addition, because the remaining dependent claims incorporate by reference all of the limitations of the corresponding independent claims, all of the dependent claims are also allowable over the cited references.

On the basis of the above amendments and remarks, reconsideration and allowance of the application is believed to be warranted, and an early action toward that end is respectfully solicited. In addition, for any issues or concerns, the Examiner is invited to call the attorney for the applicant at the telephone number provided below.

Respectfully submitted,

Paul L. Master et al.

April 18, 2005

By 

Nancy R. Gamburd
Attorney for Applicant
Registration No. 38,147
Phone: 312-876-0460
Fax: 312-2764176

CERTIFICATE OF EXPRESS MAILING

I hereby certify that the foregoing AMENDMENT AND RESPONSE UNDER 37 CFR 1.111 AND 1.115, TRANSMITTAL, FEE TRANSMITTAL, SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT, PETITION FOR EXTENSION OF TIME, CHECK NO. 1160 (in the amount of $510.00), and POSTCARD RECEIPT, for Paul L. Master et al., Serial No. 09/997,987, entitled "Apparatus, Method, System and Executable Module for Configuration and Operation of Adaptive Integrated Circuitry Having Fixed, Application Specific Computational Elements", have been deposited as Express Mail EV 464829900 US in the United States Mail, postage prepaid, addressed to the Commissioner for Patents, P.O. Box 1450, Mail Stop Fee Amendment, Alexandria, VA 22313-1450, on April 18, 2005.

Nancy R. Gamburd
Reg. No. 38,147